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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,018	08/22/2003	Zahi Said Abuhamdeh	TRA-078	1441

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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,018	ABUHAMDEH ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/14/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Texas Instruments (IEEE Std. 1149.1 (JTAG) TAP Masters with 8-bit generic host interfaces, embedded test-bus controllers; SCBS676D – December 1996-Revised August 2002) in view of Patavalis (A Brief Introduction to the JTAG Boundary Scan Interface, pages 1-6, Athens, November 8, 2001).

As per claim 1, Texas Instruments teaches an integrated circuit chip, comprising: c) an on-chip JTAG master coupled to said JTAG TAP; and d) an on-chip microprocessor interface coupled to said JTAG master (fig. 1, 3, 4, 5, pages 1-9, Texas Instruments). The examiner would like to point out that the Embedded Test Bust Controller (eTBC) in Texas Instruments is similar to JTAG master.

However Texas Instruments does not explicitly teach the specific use of a) core logic; b) an on-chip JTAG TAP coupled to said core logic.

Patavalis in an analogous art teaches JTAG Boundary Scan Interface Architecture in fig. 1 that includes core logic connected to JTAG TAP (page 2, Patavalis). Patavalis teaches that all the signals between the chip's core logic and the pins are intercepted by a serial scan path (page 2, Patavalis).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Texas Instruments' document with the teachings of Patavalis by including an additional step of using a) core logic; b) an on-chip JTAG TAP coupled to said core logic.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a) core logic; b) an on-chip JTAG TAP coupled to said core logic would provide the opportunity to access and control the signal-levels on the pins of a digital circuit and test the internal circuitry on the chip.

- As per claim 2, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teach the chip, further comprising: e) a plurality of registers coupled to said microprocessor interface and to said JTAG master (pages 12, 16, Texas Instruments).

- As per claim 3, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teach the chip, wherein: said plurality of registers includes a TDI FIFO, a TMS FIFO, a TDO FIFO, and a counter register (pages 12, 16, 24, 25, Texas Instruments).

- As per claim 4, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teach the chip, wherein: said plurality of registers includes a start bit register and an end bit register (pages 14, 15, Texas Instruments).

- As per claim 5, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teach the chip, wherein: said chip has more than five pins and five of said pins are coupled to said on-chip JTAG TAP forming a JTAG interface to said chip (fig. 1, pages 1-5, Texas Instruments).

- As per claim 6, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, further comprising: e) switching means for selectively decoupling said JTAG interface from said JTAG TAP (page 13, Texas Instruments).

- As per claim 7, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said switching means is coupled to and controllable by said JTAG master (fig. 1, pages 5, 9, 13, Texas Instruments).

- As per claim 8, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said switching means couples said JTAG master to said JTAG TAP when said JTAG interface is decoupled from said JTAG TAP, and said switching means couples said JTAG interface to said JTAG TAP when said JTAG master is decoupled from said JTAG TAP (fig. 1, pages 5, 6, 9, 13, Texas Instruments).

- As per claim 9, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches an integrated circuit chip, comprising: c) an on-chip JTAG interface selectively coupled to said JTAG TAP; d) an on-chip microprocessor interface selectively coupled to said JTAG TAP; and e) switching means for selectively coupling said JTAG interface and said microprocessor interface to said JTAG TAP (fig. 1, pages 5, 6, 9, 13, Texas Instruments).

Patavalis teaches a) core logic; b) an on-chip JTAG TAP coupled to said core logic ("JTAG Boundary Scan Interface Architecture" in fig. 1, page 2, Patavalis).

- As per claim 10, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said switching means operates to decouple said JTAG interface from said JTAG TAP when said microprocessor interface is coupled to said JTAG TAP, and said switching means operates to decouple said microprocessor interface from said JTAG TAP when said JTAG interface is coupled to said JTAG TAP (fig. 1, pages 5, 6, 9, 13, Texas Instruments).

- As per claim 11, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said microprocessor interface includes a plurality of registers (pages 12, 16, Texas Instruments).

- As per claim 12, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said switching means is controllable via said microprocessor interface (fig. 1, pages 5, 9, 13, Texas Instruments).

- As per claim 13, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, further comprising: f) a switching means enable interface for receiving a signal to enable said switching means, wherein said switching means is inoperable without receiving said signal (discrete control and multiplexers in the functional block diagram on page 3, page 16, Texas Instruments).

- As per claim 14, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: in the absence of said signal said switching means decouples said microprocessor interface from said JTAG TAP and couples said JTAG interface to said JTAG TAP (fig. 1, the functional block diagram on page 3, pages 5, 6, Texas Instruments).

16, Texas Instruments).

- As per claim 15, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said plurality of registers includes a TDI FIFO, a TMS FIFO, a TDO FIFO, and a counter register (pages 12, 16, 24, 25, Texas Instruments).

- As per claim 16, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said TDI FIFO and said TMS FIFO each being N-bits in size, and said microprocessor interface includes means for performing TAP operations having bit counts in excess of N-bits (fig. 1, pages 5, 16, 24, 25, Texas Instruments).

- As per claim 17, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: means for performing TAP operations having bit counts in excess of N-bits includes means for cycling said TAP through state elements and holding it in one of four states (fig. 8, tables 7-12, pages 19-24, Texas Instruments).

- As per claim 18, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said four states include Test-logic Reset, Run-Test Idle, Pause-IR, and Pause-DR (table 12, pages 21, 23, 24, Texas Instruments).

- As per claim 19, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches an integrated circuit chip comprising: c) an on-chip JTAG master selectively coupled to said JTAG TAP; d) an on-chip JTAG interface selectively coupled to said JTAG TAP; and e) switching means for selectively coupling said JTAG master and said JTAG interface to said JTAG TAP (fig. 1, pages 5, 6, 9, 13, Texas Instruments).

Patavalis teaches a) core logic; b) an on-chip JTAG TAP coupled to said core logic ("JTAG Boundary Scan Interface Architecture" in fig. 1, page 2, Patavalis).

- As per claim 20, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said switching means operates to decouple said JTAG interface from said JTAG TAP when said JTAG master is coupled to said JTAG. TAP, and said switching means operates to decouple said JTAG master from said JTAG TAP when said JTAG interface is coupled to said JTAG TAP (fig. 1, pages 5, 6, 9, 13, Texas Instruments).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

INFORMATION DISCLOSURE CITATION

PAGE 1 OF 1

Atty Docket No. TRA-078	Serial No. 10/647,018
Applicant Zahi Abuhamdeh et al.	
Filed August 22, 2003	Group

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

2/10/06	DG	"SCANSTA 101 Low Voltage IEEE 1149.1 STA Master", Specification Rev. DS101215, National Semiconductor Inc.; October, 2002
2/10/06	DG	"IEEE Std. 1149.1 (JTAG) TAP Masters with 8-BIT Generic Host Interfaces" Embedded Test-Bus Controllers; SCBS676D-December 1996-Revised 8/2002
2/10/06	DG	"IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices", ALTERA September 2000, ver. 4.05 ; Application Note 39
2/10/06	DG	"A Brief Introduction to the JTAG Boundary Scan Interface", Nick Patavalis, Athens; November 8, 2001

EXAMINER DG Sandhu

DATE CONSIDERED 2/10/06

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